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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,633	03/22/2004	Robert Tod Dimpsey	AUS920040062US1	2625

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EXAMINER	
MOORE, PATRICK M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,633	DIMPSEY ET AL.	
	Examiner	Art Unit	
	Patrick M. Moore	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/30/05;4/11&25/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 have been examined.

Information Disclosure Statement

2. The information disclosure statements (IDS) were submitted on 30 June 2005, 11 April 2006 and 25 April 2006. The submission is in compliance with the provisions of 37 CFR 1.97, except where noted below. Accordingly, the information disclosure statements have been considered by the Examiner.

a. Within the IDS filed on **30 June 2005**, the NPL document, labeled as **BJ** in **Other Prior Art** section on **Page 2 of 4** was not considered by Examiner because they lack an English translation as required by 37 CFR 1.98(a)(3).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3, 4, 12, 14, 15 & 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. **Claims 3 & 14** each recite the limitation "the access the one byte" in Line 3. There is insufficient antecedent basis for these limitations in the claims. Examiner notes that changing the limitation to “an access to the one byte” would overcome this rejection.

b. **Claims 4, 15 & 24** recite the limitation "the subsequent memory location" in Lines 16-17, Lines 17-18 & Line 19, respectively. There is insufficient antecedent basis for these limitations in the claims.

c. **Claim 12** recites the limitation "the method" in Line 3. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 23-26 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. As defined on page 59 of Applicant's Specification, a computer readable medium, which includes radio frequency waves and wireless communication links, constitutes non-statutory subject matter. A transmission-type medium, as claimed by applicant, does not fall within any of the patent eligible categories set forth by 35 U.S.C. 101: process, machine, manufacture or composition of matter. As set forth in 1 Chisum, Sec. 1.02[3] (citing W. Robinson, The Law of Patents for Useful Inventions 270 (1890)), a product is a tangible physical article or object, some form of matter, which a signal is not. That the other product classes require physical matter is evidence that a manufacture was also intended to require physical matter. A signal or carrier wave, as a form of energy, does not

fall within the definition of process, machine, manufacture or composition and therefore does not fall within one of the four statutory classes of Sec. 101.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-8, 10-19 & 21-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Hervin et al (US Patent # 5,805,879), herein Hervin.

a. **As for Claim 1**, FROG discloses a method in a data processing system for generating coverage data for accesses to dynamically allocated data during execution of code in a data processing system **[Column 1, Lines 16-22]**, the method comprising: responsive to a request to dynamically allocate a memory area for dynamically allocated data, dynamically allocating the memory area **[Column 3, Lines 53-56]**; responsive to dynamically allocating the memory area, associating the memory area with a data access indicator **[Column 3, Line 66 – Column 4, Line 10]**; responsive to executing an instruction in the code at a processor in the data processing system, determining whether an access to a memory location associated with the data access indicator has occurred **[Figure 7, #715 & Column 4, Lines 24-44]**; and if the data access indicator is associated with the memory area, changing a state of the data access indicator by the

processor when the instruction is executed **[Figure 7, #730]**, wherein the coverage data for the dynamically allocated data is generated during execution of the code by the processor **[Column 11, Line 55 – Column 12, Line 11]**.

b. **As for Claim 2**, FROG further discloses the method of claim 1, wherein the data access indicator includes an identification of a starting location and an ending location for the memory location allocated **[Column 2, Line 62 – Column 3, Line 7]**.

c. **As for Claim 3**, FROG further discloses the method of claim 2, wherein the data access indicator includes the identification of one byte beyond the ending location and wherein the access the one byte beyond the ending location indicates that a memory size of the memory area is insufficient **["Specified location within the segment" in Column 4, Lines 4-10]**. *Examiner understands that an offset of "one byte" beyond would be an inherent unit for loading into the address pointer disclosed by Hervin.*

d. **As for Claim 4**, FROG further discloses the method of claim 1, wherein the memory area includes a starting memory location **["Base address" in Column 3, Line 1]**, an ending memory location **["Base address... and an offset" in Column 3, Lines 1-3]** in which the starting memory location and the ending memory location span a requested size of memory equal to the request **[Column 2, Line 62 – Column 3, Line 7]**, and a subsequent memory location located one byte after a ending location **["Specified location within the segment" in**

Column 4, Lines 4-10], wherein the data access indicator is a first data access indicator in a set of data access indicators associated with the memory area, wherein the first data access indicator is associated with the starting memory location in the memory area **["No" branch of Figure 7, #715 & Column 2, Line 62 – Column 3, Line 7]**, and wherein the associating step includes: associating a second data access indicator in the set of data access indicators with the ending location for the requested memory area **[Figure 7, #735 & Column 4, Lines 4-10]**; and associating a third data access indicator in the set of data access indicators with the subsequent memory location **[Figure 7, Column 13, Lines 4-17]**.

e. **As for Claim 5**, FROG further discloses the method of claim 1 further comprising: retrieving call stack information in response to dynamically allocating the memory area **[Column 8, Lines 35-48]**.

f. **As for Claim 6**, FROG further discloses the method of claim 5 further comprising: identifying code making the request for the memory area using the call stack information **["ID Stage" in Column 13, Lines 49-65]**.

g. **As for Claim 7**, FROG further discloses the method of claim 5 further comprising: determining calling sequences in the code using the call stack information **[Column 8, Lines 61-66]**.

h. **As for Claim 8**, FROG further discloses the method of claim 1, wherein the access indicator is located in a field in the instruction **[Figure 5, #510 & Column 11, Lines 55-67]**.

i. **As for Claim 10**, FROG further discloses the method of claim 1, wherein the access indicator associated with the instruction is located in a page table **[Column 8, Lines 49-53]**.

j. **As for Claim 11**, FROG further discloses the method of claim 1, wherein memory location accessed during execution of the code have set data access indicators set when the state of access indicators associated with an executed instruction are changed, while memory location unaccessed during execution of the code have unset data access indicators because the state of the unset data access indicators remain unchanged **[Column 4, Lines 24-44]**.

k. **As for Claim 12**, FROG discloses a data processing system for generating coverage data for accesses to dynamically allocated data during execution of code in a data processing system, the method comprising: allocating means, responsive to a request to dynamically allocate a memory area for dynamically allocated data, dynamically for allocating the memory area **[Column 3, Lines 53-5]**; associating means, responsive to dynamically allocating the memory area, for associating the memory area with a data access indicator **[Column 3, Line 66 – Column 4, Line 10]**; determining means, responsive to executing an instruction in the code at a processor in the data processing system, for determining

whether an access to a memory location associated with the data access indicator has occurred **[Figure 7, #715 & Column 4, Lines 24-44]**; and changing means for changing a state of the data access indicator by the processor when the instruction is executed if the data access indicator is associated with the memory area **[Figure 7, #730]**, wherein the coverage data for the dynamically allocated data is generated during execution of the code by the processor **[Column 11, Line 55 – Column 12, Line 11]**.

l. **Claim 13** is rejected with same rationale as Claim 2.

m. **Claim 14** is rejected with same rationale as Claim 3.

n. **Claims 15 & 25** are rejected with same rationale as Claim 4.

o. **Claims 16 & 25** are rejected with same rationale as Claim 5.

p. **Claims 17 & 26** are rejected with same rationale as Claim 6.

q. **Claim 18** is rejected with same rationale as Claim 7.

r. **Claim 19** is rejected with same rationale as Claim 8.

s. **Claim 21** is rejected with same rationale as Claim 10.

t. **Claim 22** is rejected with same rationale as Claim 11.

u. **As for Claim 23**, FROG discloses a computer program product in a computer readable medium for generating coverage data for accesses to dynamically allocated data during execution of code in a data processing system, the

computer program product comprising: first instructions, responsive to a request to dynamically allocate a memory area for dynamically allocated data, dynamically for allocating the memory area **[Column 3, Lines 53-5]**; second instructions, responsive to dynamically allocating the memory area, for associating the memory area with a data access indicator **[Column 3, Line 66 – Column 4, Line 10]**; third instructions, responsive to executing an instruction in the code at a processor in the data processing system, for determining whether an access to a memory location associated with the data access indicator has occurred **[Figure 7, #715 & Column 4, Lines 24-44]**; and fourth instructions for changing a state of the data access indicator by the processor when the instruction is executed if the data access indicator is associated with the memory area **[Figure 7, #730]**, wherein the coverage data for the dynamically allocated data is generated during execution of the code by the processor **[Column 11, Line 55 – Column 12, Line 11]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 9 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hervin et al. (US Patent # 5,805,879) as applied to claims 1 & 12 above, and further in view of Sederlund et al (US Patent # 6,647,301), herein Sederlund.

a. **Hervin** does not expressly disclose a shadow memory.

b. **However, per Claims 9 & 20**, **Sederlund** discloses the method of claim 1 and the data processing system of claim 12, wherein the access indicator associated with the instruction is located in a shadow memory **[Column 25, Lines 46-64]**.

c. **Hervin** *and* **Sederlund** *are analogous art because they are from the same field of endeavor: computer memory control techniques. At the time of invention, it would have been obvious for one of ordinary skill in the art to combine the memory access indicator, as disclosed by* **Hervin**, *with the Shadow Memory, as disclosed by* **Sederlund**. *Furthermore, the suggestion/motivation for doing so would have been for the benefit of ensuring data accuracy, which is critical in a dynamically allocated memory system. Furthermore,* **Sederlund** *teaches the benefits of using a Shadow Memory in a memory system in* **Column 13, Lines 35-47**.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick M. Moore whose telephone number is (571) 272-1239. The examiner can normally be reached on M-F 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabahn can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 5/12/06

PMM

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SUPERVISORY PATENT EXAMINER